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EMPIRICAL DEMONSTRATION OF NEXT GENERATION HIGH SPEED HYBRID CMOS-SET BASED CONSUMER FRIENDLY IBM MACHINE SUBSECTION

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ABSTRACT

At the very dawn of post CMOS era Single Electronics ushered new ventures in resolving power dissipation and power consumption like hindrances. Low power consuming, high speed & high integration density Single Electronics play a major role in modern nano scale electronics. It schematically focus on the movement and position of a single electron. There has been extensive research to develop specific applications of Single Electronics in Defense applications (for unmanned and remote areas), Space Technologies (such as space vehicles), medical applications (such as space-maker battery) etc. The research criteria in such applications are minimum power for maximum battery lifetime. One such revealation of implementation of Single Electronics is and the consequences are analysized to compare it with conventional technologies.

KEYWORDS: CMOS, ITRS, SET, Hybrid CMOS-SET, IBM machine subsections.

INTRODUCTION

The fundamental topology of device research is down scaling of device sizes . The decisive factors in down scaling are i)what would be the minimum gate length ii) What would be the minimum gate oxide thickness iii) What would be the minimum band gap etc [1-6].

Sir Gorden E. Moore, in connection to such findings stated that - the number of transistor that can be fit in single die area doubles within every 18months [7]. Such trend in device down scaling stimulated electronic industry to produce high speed low power consuming ultra dense digital circuits. But the fragility is that such down scaling is not a 'Never ending process'. The power dissipation factor proportionally increases with the down scaling of the device sizes. Thus constant device down scaling will increase temperature manifold which might be equal to the temperature of surface of Sun. Besides power dissipation is an avoidable circumstances. Other hindrances of continuous down scaling are short channel effects, leakage phenomena and performance degradation. Thus the rendering of down scaling is somehow subjected to technological limitation. The same has been observed by the statement made by Gorden E. Moore in late 2003. Also International Technology for Road Map of Semiconductor (ITRS) suggested in the same fashion about the device miniaturization in 2005 [8]. Thus the concept of the 'more to Moore' technology attracted researchers worldwide in post CMOS era.

The extensive sophisticated advanced e-beam lithography technique augmented the device minimization manifold. Apparently, this brought technological sifting in effect. The new technology evoked in the context of post CMOS era are i)Carbon Nano Tube ii)Resonant Tunneling Diode iii)RFSQ iv)Quantum Electronic Device [9-12]. Quantum electronics plays an imperative role in designing next generation digital electronics. Quantum structure is excessively referred in both industry and academia owing to its unmatched credentials in device minimizing. But amid its numerous advantages over other consumer electronics, it faces major challenges like technological limitations, structure related limitation, material related limitation, process related limitation etc [13]. In such context device research coherently progressed to single electron transistor technology based on the tunnel phenomena of electrons. This phenomena is considered to be pivotal as tunneling leads to extreme manipulation of electrons in a confined region- it is attributed as the ultimate form of device research.

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Thus Researchers attempted SET technology for next generation device modeling. The following section will briefly outline SET and it's methodology, some of the operational aspects of SET, few drawbacks of SET and some relevant options to resolves such drawbacks. Subsequently, the authors here propose a nano device modeling of a high valued digital logic circuit which are quite substantial and can be incorporated in IBM machines. A comparative study is also concluded at the last section of this letter to outline the modulus operandi of the stated model.

SET IN BRIEF

SET evolved as a promising elementary device that insights the charge transport phenomena. The nature of charge transport is discrete unlike other conventional devices. It comprises of two tunnel junctions that share a common electron as depicted in the fig.1 below.

The fig.1 reveals control flow of current as the SET is brought into active region. The Coulomb energy plays an impetus role ensuring proper control flow from source to drain. The tunnel junction is a composite structure of two pieces of metal, amid which a thin layer of insulator is sandwiched having thickness of 1 nm [14-17].

Electrons can granule from one side of the electrodes to the other side if and only if the coulomb energy is greater than the static energy given by $E_c = \frac{e^2}{2C} > KT$ (1)

Where K=Boltzmann constant=1.38×10^{-34}J/K, T= absolute temperature. Thus, tunneling is discrete process ;the flow of electrons increases manifold (multiple of 'e's) through the tunnel junction. Here the bias voltage is less than coulomb gap voltage and if the gate voltage enhances in such situation, the energy of the initial system proportionately increases. Thereby, the energy of the system on the island gradually will diminish. One can determine the coulomb energy as the prerequisite charge of an island with electrons. The tunnel junctions are channeled to mobilize the electron independently from island to island. One interesting criteria is that the electron are strictly localized on the island and tunnel resistance is sufficiently large enough over the fundamental resistance i. e.

$$R > R_q = h/e^2 \quad (2)$$

It was empirically demonstrated by Likharev [18] that the gate voltage is critical to the corresponding slope on coulomb staircase. The quantum dots interface with the source and drain of SET electrons. The potential drop in the dot is manipulated by the gate electrons which is eventually coupled to the quantum dot (Q_d). It ensures that when current is zero, the number of electron becomes fixed. Thereby the essential operation of SET device ensures that the tunnel junction resistance has to be greater than the quantum resistance and the charging energy i.e., quantum dot capacitance has to be larger than avoidable formal energy. It is given by

$$\mathbf{C_T = C_G + C_D + C_S} \quad (3)$$

Where C_G=Gate capacitance, C_D=Drain capacitance, C_S=Source capacitance, C_T=Total capacitance. To simulate the tunneling phenomena one has to determine the rate of all possible tunneling events. Once tunneling occurs the circuit is free from energy changes. The co-relation between free energy 'F', electrostatic energy 'U', work done 'W ' is given by $F = U - W$ (4)

IF SET IS THE ALTERNATIVE THEN WHAT RESTRICT ITS INCORPORATION

The Researchers intend to scale down the computer chip rapidly, thus the idea of incorporating SETs has increased manifold. Like several other electronics devices SET insights the potential to reach the molecular scale and would confine it-self in far less space as compared to the conventional counterpart. The small size, fast inaction and low power dissipation of SET circuits make them potentially useful and best compliment for next generation IC design.

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But amid all the intrinsic limitations are deliberately restricting its maximal employment in digital electronics. Researchers in their proposed study revealed few of them. Among other disadvantages, low gain, random background charge and room temperature operation stands to be extremely catastrophic. Thus an alternative was intended.

Hybrid CMOS-SET ushered new horizons in replacing CMOS. Besides it is a bridging element between CMOS and SET. Thus Researchers tend towards this promising alternative. Hybrid CMOS-SET circuits have been reported in many journals [19-21]. The authors have corroborated the same for next zen device design. Few Hybrid CMOS-SET based logic realizations have been enumerated here for perusal.

REVIEW OF IBM MACHINES

The IBM machines popularized as a composite structure of several combinational logic circuits. With the incorporation of excellent logical mechanism IBM distinguished themselves as the pioneer of electronics industry since long. Here the authors considered a simple logic circuit; the same is often used in IBM machines. Interestingly, the verification combination for checking two Boolean networks consecutively is represented using functional equivalence circuits. Topologically their performance amends due to technological development of optimization, although it has to reflect the same behavior as in before. Many published articles do resemble many methods that has been proposed efficiently and satisfactorily. Here the authors propose a novel architecture used by IBM machines, the same CMOS based circuit has been realized magnificently as a serial adder in many of their application.

PROPOSED MODEL

The circuit realized in Fig4 is capable to perform arithmetic and logic operations and the same can be integrated into a nano scaled IC which can be fitted to any present day available real time systems. When digital signals are transmitted from one point to another a noise impulse is created and that changes the logic level of the data bit.

The circuit comprises of 5 hybrid CMOS-SET based AND gates 3 hybrid CMOS-SET based OR gates and one hybrid CMOS-SET Inverter. The AND gates A1,A2,A3,A4 along with the OR gates O1,O2,O3 gives and output that equals to

C out =A.B+B.Ci+A.Ci

This output is driven to OR gates O2 through a hybrid CMOS-SET Inverter circuit. Thus OR gates also receives the signal A, B, Ci for AND gate-A4. The output of this gates is given to AND –gate-A5 , which receives its second input for OR –gate-O1. Output of AND gate A5 output of AND-gate-O5 is sum output. So we obtain

$S_n = (\mathrm{A}+\mathrm{B}+C_i)\ (\overline{A.C\imath + B.C\imath + A.B + A.B.C\imath})$

$S_n = (\mathrm{A}+\mathrm{B}+C_i)\ (\overline{A.C\imath + B.C\imath + A.B + A.B.C\imath})$

$= (\mathrm{A}+\mathrm{B}+\mathrm{Ci})\ [(\bar{A}+\bar{C\imath})(\bar{B}+\bar{C\imath})(\bar{A}+\bar{B}) + (\mathrm{A.B.}C_i)]$

$= (\mathrm{A}+\mathrm{B}+\mathrm{C_i})\ (\bar{A}.\bar{B} + \bar{A}.\bar{C} + \bar{A}.\bar{B}.\bar{C} + \bar{B}.\bar{C\imath} + \mathrm{A.B.C})$

$= \mathrm{A}.\bar{B}.\bar{C\imath} + \mathrm{A.B.Ci} + \bar{A}.\mathrm{B}.\bar{C}i + \bar{A}.\bar{B}.C$

From the Fig-4 it is evident that electron from input to output is manipulated by intrinsic properties of hybrid CMOS-SET itself at different block interval with the incorporation of input signal.

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As a consequence the propagation delay is controlled which minimizes the power dissipation of the proposed architecture, resulting high integration density of the model. Evidently, the robustness and the high performance increased its acceptability for IC configuration .

Tables: ***Emperical study of power dissipation and power consumption of different device in the proposed phototype of IBM Machine***

Gate	Power Consumption	No. of CMOS	No. of SET
AND	0.01V	3	3
OR	0.01V	3	3
NOT	0.01V	1	1

CONCLUSION

The authors here successfully presented a novel architecture of next generation advanced arithmetic circuit using Hybrid CMOS-SET. The perfect combination essentially delivers high speed output. Two main substantial heights have been achieved- 1) high speed low power consuming arithmetic circuit and 2) extremely fast computational speed. Hereby the authors conclude that such composition can be adhered for other sophisticated complex circuits.

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List of figure

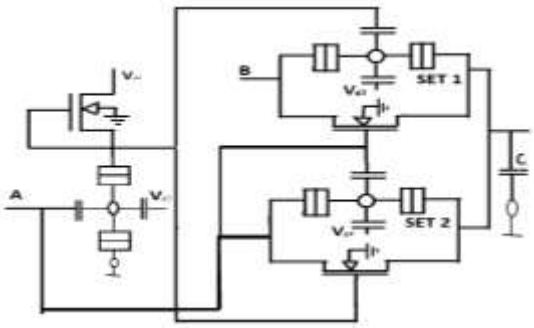

Fig1. Hybrid CMOS-SET based AND realization

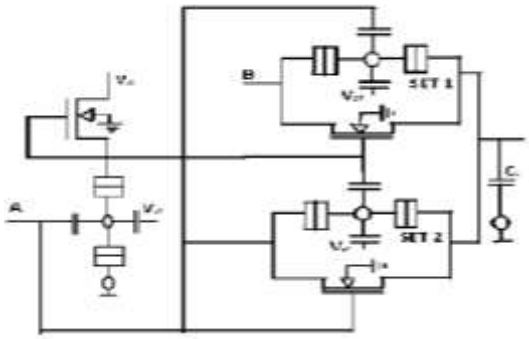

Fig 2. . Hybrid CMOS-SET based OR realization

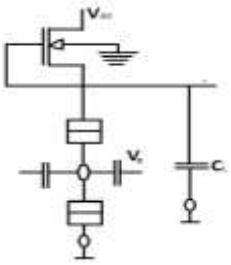

Fig 3. Hybrid CMOS-SET based NOT realization

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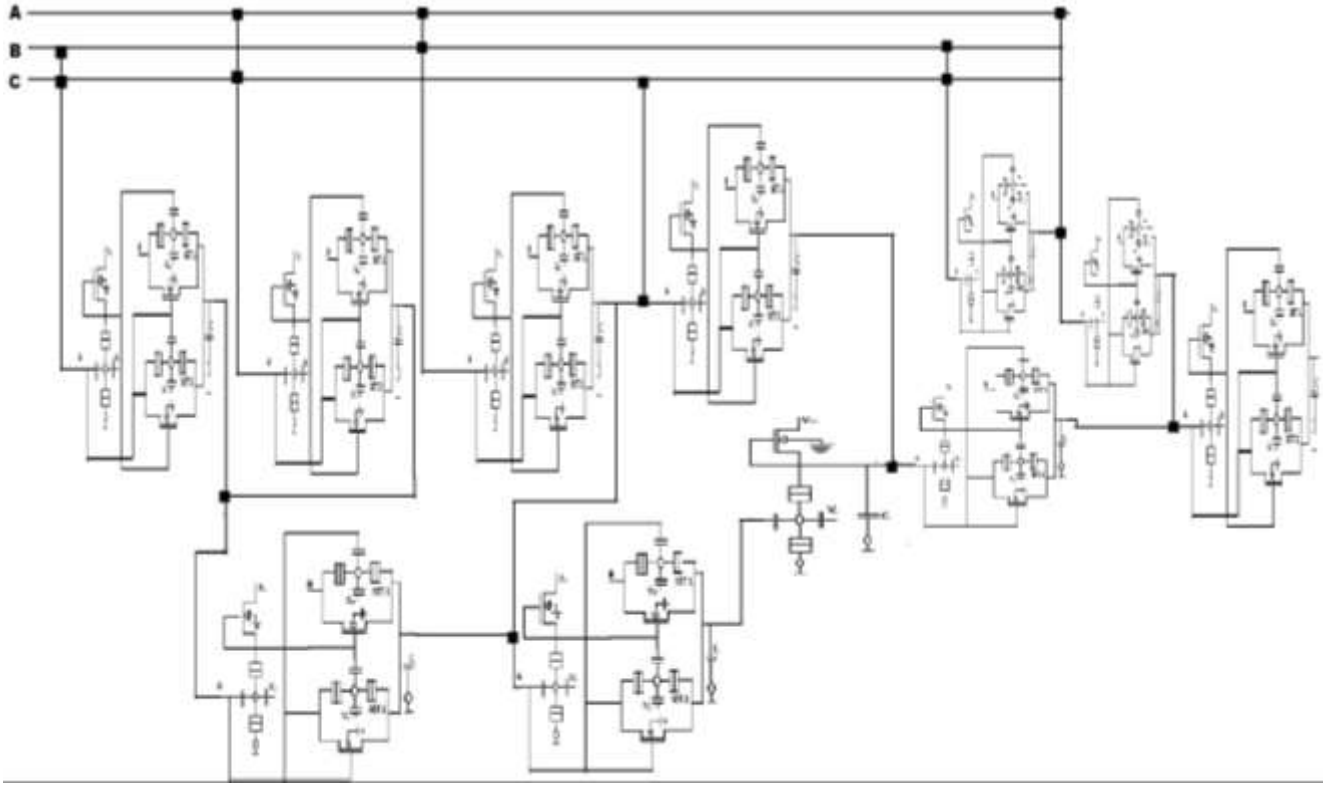

Fig 4. Hybrid CMOS-SET based IBM Machine Prototype